Dc Shell User Guide

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Dc Shell User Guide
Dc Shell User Guide Online Library Dc Shell User Guide dc_shell. The dc_shell supports two scripting languages – dcsh, which uses the Synopsys language, and dctcl, which uses Tcl (Tool Command Language). It is recommended that Design Analyzer be used for most of the synthesis and optimization processes.

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Get Free Dc Shell User Guide optimization processes. The dc_shell is preferable for a standardized synthesis methodology or optimization of large designs. Synopsys Design Compiler Tutorial - homepages.cae.wisc.edu unix> dc_shell-t. Step 1. Setup technology library. To synthesize a design you need technology library which will contain description of

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Design Analyzer and a command line interface call dc_shell. The dc_shell supports two scripting languages – dcsh, which uses the Synopsys language, and dctcl, which uses Tcl (Tool Command Language). It is recommended that Design Analyzer be used for most of the synthesis and optimization processes. The dc_shell is preferable for a standardized synthesis methodology or optimization of large designs.

Synopsys Design Compiler Tutorial - CAE Users
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For more information on the compile ultra command consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compile ultra at the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints.

RTL-to-Gates Synthesis using Synopsys Design Compiler
dc_shell-topo> compile_ultra -gate_clock -no_autoungroup # The compile_ultra command may take a while! dc_shell-topo> change_names -rules verilog -hierarchy dc_shell-topo> write -format ddc -hierarchy -output gcdGCDUnit_rtl.mapped.ddc dc_shell-topo> write -f verilog -hierarchy -output gcdGCDUnit_rtl.mapped.v

RTL-to-Gates Synthesis using Synopsys Design Compiler
%> dc shell –t any memory LIB file %> dc_shell dc_shell-t> read_lib t13spsram512x32_slow_syn.lib dc_shell-t> write_lib t13spsram512x32 -output \ t13spsram512x32_slow_syn.db Modify <.synopsys_dc.setup> File: "* user library name, which should be the same as the library name in the Artisan set link_library slow.db t13spsram512x32_slow.db

Training Course of Design Compiler [□□□□]
dc_shell –f scriptFile Most efficient and common usage is to put TCL commands into scriptFile ,including "quit" at the end TCL = Tool Command Language Edit and rerun scriptFile as needed GUI version (Design Vision) design_vision From dc_shell: gui_start Main advantage over dc_shell is to view the synthesized schematic

Automated Synthesis from HDL models
For use in dc_shell-t (Tcl mode of dc_shell) only. string acs_get_parent_partition design_name [-hierarchy] [-list] acs_get_path (dctcl-mode only) Gets the path location for the specified file. To specify a file, specify its file type and, for pass-dependent files, its pass directory. For use in dc_shell-t (Tcl mode of dc_shell) only. string acs_get_path

Synthesis Quick Reference - Computer Science
Design Compiler Graphical extends DC Ultra™ topographical technology to produce physical guidance to the IC Compiler place-and-route solution, tightening timing and area correlation to 5% while speeding-up IC Compiler placement by 1.5X.

Design Compiler Graphical - Synopsys
Both the "dc_shell" and it's GUI will pop up and look something like this: 4) Click on File->Setup to verify that the parameters setup in the "synopsys_dc.setup" file have taken effect (look through both tabs to see all the variables and parameters setup). You should see the following in your screen: Link Library: osu05_stdcells.db

ECE 128 Synopsys Tutorial: Using the Design Compiler ...
unix> dc_shell-t. Step 1. Setup technology library. To synthesize a design you need technology library which will contain description of the cells from the fab, and their timing. This is usually a .db file found in library installation directory. To do this 1(a). Tell synopsys where your <library>.db file is.

dc_shell.html - Ip
the compileultracommand consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileultraat the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints. DC considers two

RTL-to-Gates Synthesis using Synopsys Design Compiler
For more information on the compile command consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileat the DC shell prompt. Run the following command and take a look at the output. dc_shell-xg-t> compile -map_effort medium -area_effort medium The compile command will report how the design is being optimized.

RTL-to-Gates Synthesis using Synopsys Design Compiler
output from a shell command back into dc_shell (i.e. there is nothing analogous to using backquote in the shell for command substitution) 5 . You might think that you could set an environment variable in sh, and then use get_unix_variableto

My Favorite dc shell Tricks
Comments? E-mail your comments about Synopsys documentation to doc@synopsys.com HDL Compiler for Verilog Reference Manual Version 2000.05, May 2000

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